**实验报告**

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| 专业 | 软件工程 | | 课程名称 | 计算机组成原理课程设计 | |
| 任课老师 | 仇建 | 指导老师 | 仇建 | 机位号 |  |
| 实验序号 | 1 | 实验名称 | 多功能ALU设计实验 | | |
| 实验时间 |  | 实验地点 |  | 实验设备号 |  |
| **一、实验程序源代码** | | | | | |
| 程序源代码  module Module(ALU\_OP,AB\_SW,F\_LED\_SW,LED);  input [2:0]ALU\_OP;  input [2:0]AB\_SW;  input [2:0]F\_LED\_SW;  output [7:0]LED;  //  reg [31:0]A,B;  wire [2:0]AB\_SW;  //  reg [31:0]F;  reg C32;  reg [7:0]LED;  wire OF;  reg ZF;  wire [2:0]F\_LED\_SW;  //  always @(\*)  begin  case(AB\_SW) //  3'b000:begin A=32'h0000\_0000;B=32'h0000\_0000;end  3'b001:begin A=32'h0000\_0003;B=32'h0000\_0607;end  3'b010:begin A=32'h8000\_0000;B=32'h8000\_0000;end  3'b011:begin A=32'h7FFF\_FFFF;B=32'h7FFF\_FFFF;end  3'b100:begin A=32'hFFFF\_FFFF;B=32'hFFFF\_FFFF;end  3'b101:begin A=32'h8000\_0000;B=32'hFFFF\_FFFF;end  3'b110:begin A=32'hFFFF\_FFFF;B=32'h8000\_0000;end  3'b111:begin A=32'h1234\_5678;B=32'h3333\_2222;end  default:begin A=32'h9ABC\_DEF0;B=32'h1111\_2222;end  endcase  end  always @(\*)  begin  case(ALU\_OP)  3'b000:begin F<=A&B; end  3'b001:begin F<=A|B; end  3'b010:begin F<=A^B; end  3'b011:begin F<=~(A|B); end  3'b100:begin {C32,F}<=A+B; end  3'b101:begin {C32,F}<=A-B; end  3'b110:begin if(A<B) F<=32'h0000\_0001; else F<=32'h0000\_0000; end  3'b111:begin F<=B<<A; end  default:begin F<=32'h0000\_0000; end  endcase  end  always @(\*)  //ZF  begin  if(F==32'h0000\_0000)  ZF<=1;  else  ZF<=0;  end  //OF  assign OF = A[31]^B[31]^F[31]^C32;  //  always @(\*)  begin  case(F\_LED\_SW)  3'b000:LED=F[7:0];  3'b001:LED=F[15:8];  3'b010:LED=F[23:16];  3'b011:LED=F[31:24];  default:begin LED[7]=ZF;LED[0]=OF;LED[6:1]=6'b0; end  endcase  end  endmodule  仿真代码  module Test;  // Inputs  reg [2:0] ALU\_OP;  reg [2:0] AB\_SW;  reg [2:0] F\_LED\_SW;  // Outputs  wire [7:0] LED;  // Instantiate the Unit Under Test (UUT)  Module uut (  .ALU\_OP(ALU\_OP),  .AB\_SW(AB\_SW),  .F\_LED\_SW(F\_LED\_SW),  .LED(LED)  );  initial begin  // Initialize Inputs  ALU\_OP = 0;  AB\_SW = 0;  F\_LED\_SW = 0;  // Wait 100 ns for global reset to finish  #100;    // Add stimulus here  ALU\_OP=3'b000;AB\_SW=3'b000;F\_LED\_SW=3'b011;  #100;  ALU\_OP=3'b001;AB\_SW=3'b001;F\_LED\_SW=3'b010;  #100;  ALU\_OP=3'b010;AB\_SW=3'b010;F\_LED\_SW=3'b001;  #100;  ALU\_OP=3'b100;AB\_SW=3'b100;F\_LED\_SW=3'b000;  #100;  ALU\_OP=3'b101;AB\_SW=3'b101;F\_LED\_SW=3'b011;  #100;  ALU\_OP=3'b110;AB\_SW=3'b110;F\_LED\_SW=3'b010;  #100;  ALU\_OP=3'b111;AB\_SW=3'b111;F\_LED\_SW=3'b001;  end    endmodule | | | | | |
| **二、仿真波形** | | | | | |
| ISim (O.87xd) - [Default.wcfg] | | | | | |
| **三、电路图** | | | | | |
| ISE Project Navigator (O.87xd) - C:\Users\kannaduki\Desktop\ISE\Program3\Program3.xise - [Module (RTL1)]  ISE Project Navigator (O.87xd) - C:\Users\kannaduki\Desktop\ISE\Program3\Program3.xise - [Module (RTL1)] | | | | | |
| **四、引脚配置（约束文件）** | | | | | |
| NET "ALU\_OP[0]" LOC = T5;  NET "ALU\_OP[1]" LOC = V8  NET "ALU\_OP[2]" LOC = U8;  NET "AB\_SW[0]" LOC = N8;  NET "AB\_SW[1]" LOC = M8;  NET "AB\_SW[2]" LOC = V9;  NET "F\_LED\_SW[0]" LOC = T9;  NET "F\_LED\_SW[1]" LOC = T10;  NET "F\_LED\_SW[2]" LOC = B8;  NET "LED[0]" LOC = T11;  NET "LED[1]" LOC = R11;  NET "LED[2]" LOC = N11;  NET "LED[3]" LOC = M11;  NET "LED[4]" LOC = V15;  NET "LED[5]" LOC = U15;  NET "LED[6]" LOC = V16;  NET "LED[7]" LOC = U16; | | | | | |
| **五、思考与探索** | | | | | |
| 2.不能。 stl、sra、sllv、srlv、srav、jr、addi、addiu、lui、lw、sw、bwq、bne、slti、j、jal  3. 不能。  4.  ① assign SF = F[31]  ② assign PF = 1 ^ F[0] ^ F[1] ^ F[2] ^ F[3] ^ F[4] ^ F[5] ^ F[6] ^ F[7] ^ F[8] ^ F[9] ^ F[10] ^ F[11] ^ F[12] ^ F[13] ^ F[14] ^ F[15] ^ F[16] ^ F[17] ^ F[18] ^ F[19] ^ F[20] ^ F[21] ^ F[22] ^ F[23] ^ F[24] ^ F[25] ^ F[26] ^ F[27] ^ F[28] ^ F[29] ^ F[30] ^ F[31]  ③ if(ALU\_OP == 3'b100)  CF <= C32;  else  CF <= ~C32;  5.  F <= A >> B  F <= A>>>B | | | | | |
| **六、意见和建议** | | | | | |
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